MJE18004D2

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

The MJE18004D2 is state−of−art High Speed High gain BIPolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window.

It’s characteristics make it also suitable for PFC application.

Features

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector−Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- “6 Sigma” Process Providing Tight and Reproductible Parameter Spreads
- Pb−Free Package is Available*

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector−Base Breakdown Voltage	V_{CBO}	1000	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter−Base Voltage	V_{EBO}	12	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C I_{CM}	5 10	Adc
Base Current − Continuous − Peak (Note 1)	I_B I_{BM}	2 4	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	W W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.65	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

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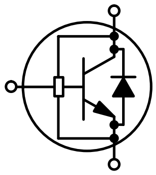
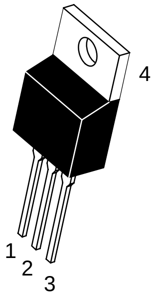
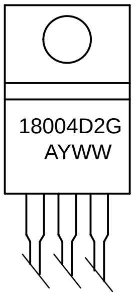
POWER TRANSISTORS
5 AMPERES,
1000 VOLTS, 75 WATTS





TO−220AB
CASE 221A
STYLE 1

MARKING DIAGRAM



18004D2 = Device Code
G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
MJE18004D2	TO−220AB	50 Units / Rail
MJE18004D2G	TO−220AB (Pb−Free)	50 Units / Rail

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Collector−Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)				$V_{CEO(sus)}$	450	547	−	Vdc
Collector−Base Breakdown Voltage (I_{CBO} = 1 mA)				V_{CBO}	1000	1100	−	Vdc
Emitter−Base Breakdown Voltage (I_{EBO} = 1 mA)				V_{EBO}	12	14	−	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)				I_{CEO}	−	−	100	µAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)			@ T_C = 25°C @ T_C = 125°C	I_{CES}	−	−	100 500	µAdc
(V_{CE} = 500 V, V_{EB} = 0)			@ T_C = 125°C				100	
Emitter−Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)				I_{EBO}	−	−	100	µAdc
ON CHARACTERISTICS								
Base−Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)			@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$	−	0.8 0.7	1 0.9	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)			@ T_C = 25°C @ T_C = 125°C		−	0.9 0.8	1 0.9	
Collector−Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)			@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$	−	0.38 0.55	0.5 0.75	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)			@ T_C = 25°C @ T_C = 125°C		−	0.45 0.75	0.75 1	
(I_C = 0.8 Adc, I_B = 40 mAdc)			@ T_C = 25°C @ T_C = 125°C		−	0.9 1.6	1.5	
(I_C = 1 Adc, I_B = 0.2 Adc)			@ T_C = 25°C @ T_C = 125°C		−	0.25 0.28	0.5 0.6	
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1 Vdc)			@ T_C = 25°C @ T_C = 125°C	h_{FE}	15 10	28 14	−	−
(I_C = 2 Adc, V_{CE} = 1 Vdc)			@ T_C = 25°C @ T_C = 125°C		6 4	8 6	−	
(I_C = 1 Adc, V_{CE} = 2.5 Vdc)			@ T_C = 25°C @ T_C = 125°C		18 14	28 20	−	
DYNAMIC SATURATION VOLTAGE								
Dynamic Saturation Voltage: Determined 1 µs and 3 µs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 Adc I_{B1} = 100 mA V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$	−	9 16	−	V
		@ 3 µs	@ T_C = 25°C @ T_C = 125°C		−	3.1 9	−	
	I_C = 2 Adc I_{B1} = 0.4 A V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C @ T_C = 125°C		−	11 18	−	
		@ 3 µs	@ T_C = 25°C @ T_C = 125°C		−	1.4 8	−	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS							
Forward Diode Voltage (I_{EC} = 1 Adc)		@ T_C = 25°C @ T_C = 125°C	V_{EC}	–	0.96 0.72	1.5	V
(I_{EC} = 2 Adc)		@ T_C = 25°C @ T_C = 125°C		–	1.15 0.8	1.7	
Forward Recovery Time (I_F = 0.4 Adc, di/dt = 10 A/µs)		@ T_C = 25°C	t_{fr}	–	440	–	ns
(I_F = 1 Adc, di/dt = 10 A/µs)		@ T_C = 25°C		–	335	–	
(I_F = 2 Adc, di/dt = 10 A/µs)		@ T_C = 25°C		–	335	–	
DYNAMIC CHARACTERISTICS							
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			f_T	–	13	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)			C_{ob}	–	60	100	pF
Input Capacitance (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			C_{ib}	–	450	750	pF
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 µs)							
Turn−on Time	I_C = 2.5 Adc, I_{B1} = 0.5 Adc I_{B2} = 1 Adc V_{CC} = 250 Vdc	@ T_C = 25°C	t_{on}	–	500	750	ns
Turn−off Time		@ T_C = 25°C	t_{off}	1.1	–	1.4	µs
Turn−on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 1 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}	–	100 150	150	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}	–	1.15 1.6	1.3	µs
Turn−on Time	I_C = 2.5 Adc, I_{B1} = 0.5 Adc I_{B2} = 0.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}	–	120 500	150	ns
Turn−off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}	1.85	– 2.6	2.15	µs
SWITCHING CHARACTERISTICS: Inductive Load (V_{CC} = 15 V)							
Fall Time	I_C = 2.5 Adc I_{B1} = 500 mAdc I_{B2} = 500 mAdc V_Z = 350 V L_C = 300 µH	@ T_C = 25°C @ T_C = 125°C	t_f	–	130 300	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	–	2.12 2.6	2.4	µs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c	–	355 750	500	ns
Fall Time	I_C = 2 Adc I_{B1} = 400 mAdc I_{B2} = 400 mAdc V_Z = 300 V L_C = 200 µH	@ T_C = 25°C @ T_C = 125°C	t_f	–	95 230	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	2.1	 2.9	2.4	µs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c	–	300 700	450	ns
Fall Time	I_C = 1 Adc I_{B1} = 100 mAdc I_{B2} = 500 mAdc V_Z = 300 V L_C = 200 µH	@ T_C = 25°C @ T_C = 125°C	t_f	–	70 100	90	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	–	0.7 1.05	0.9	µs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c	–	75 160	120	ns

TYPICAL STATIC CHARACTERISTICS

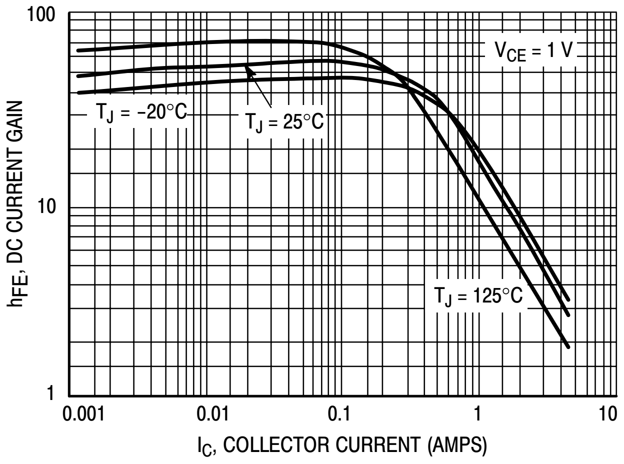


Figure 1. DC Current Gain @ 1 Volt

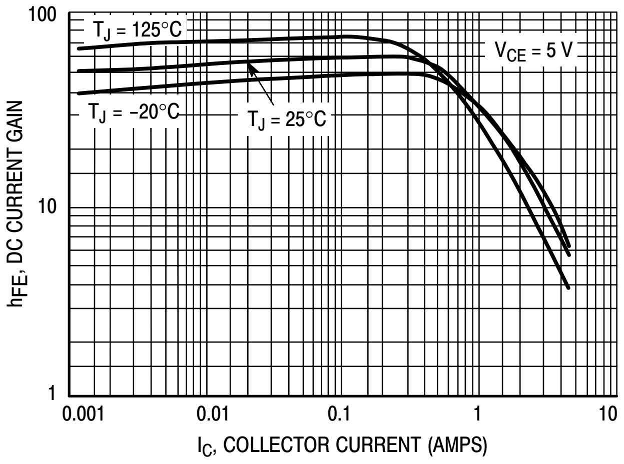


Figure 2. DC Current Gain @ 5 Volt

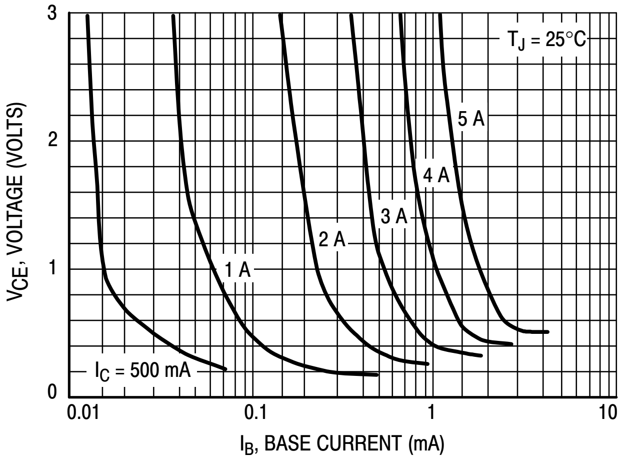


Figure 3. Collector Saturation Region

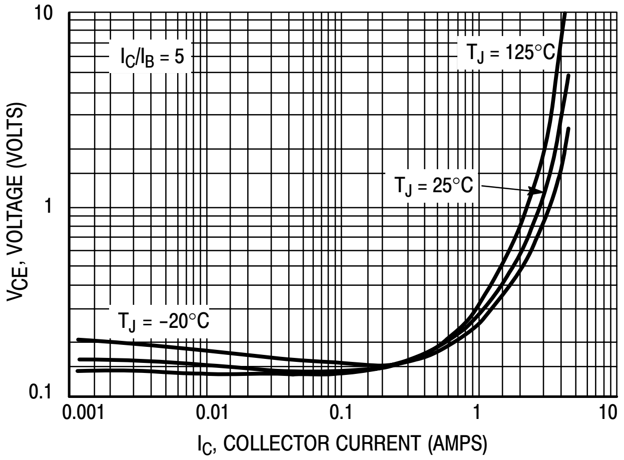


Figure 4. Collector−Emitter Saturation Voltage

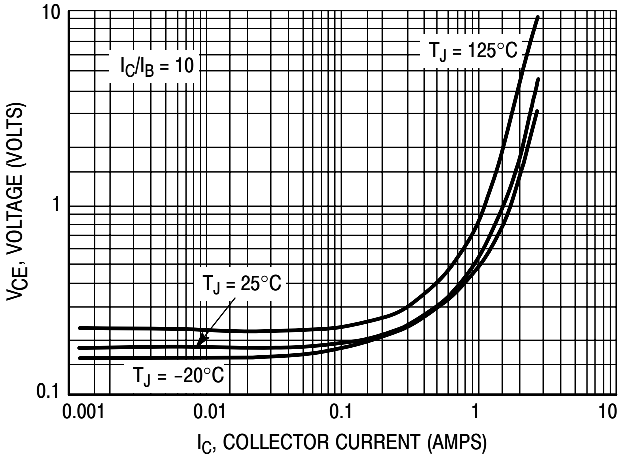


Figure 5. Collector−Emitter Saturation Voltage

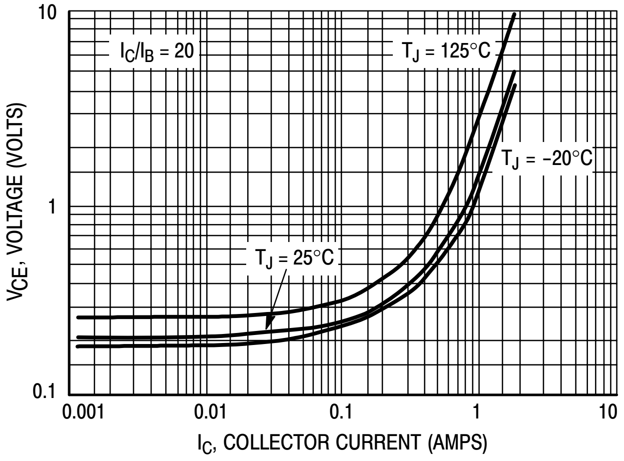


Figure 6. Collector−Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

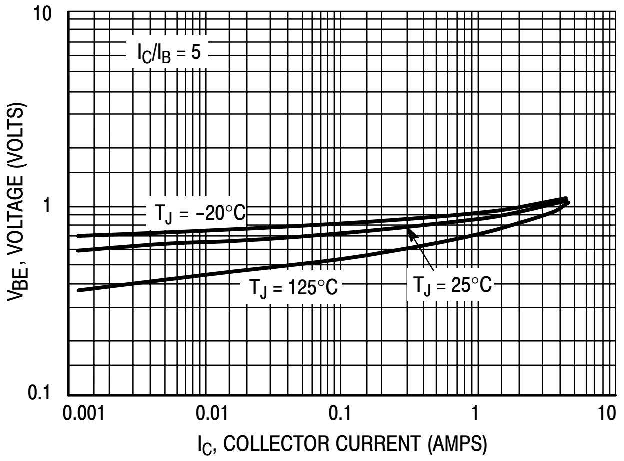


Figure 7. Base−Emitter Saturation Region

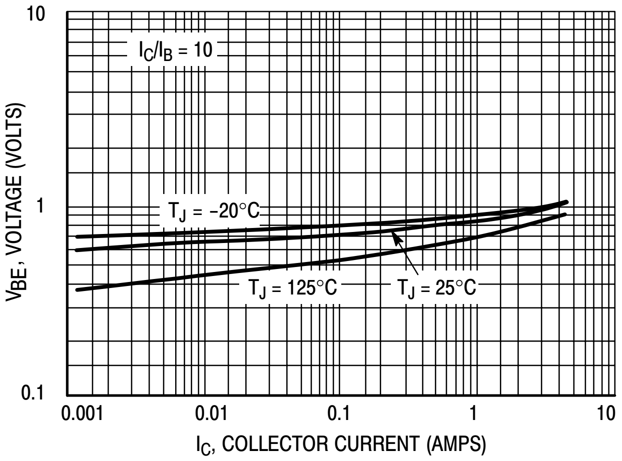


Figure 8. Base−Emitter Saturation Region

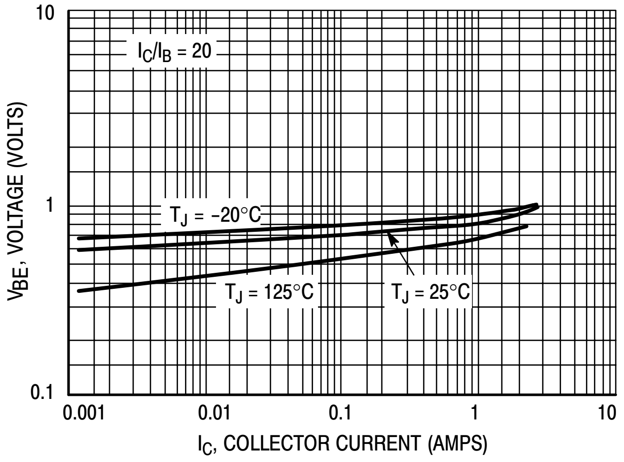


Figure 9. Base−Emitter Saturation Region

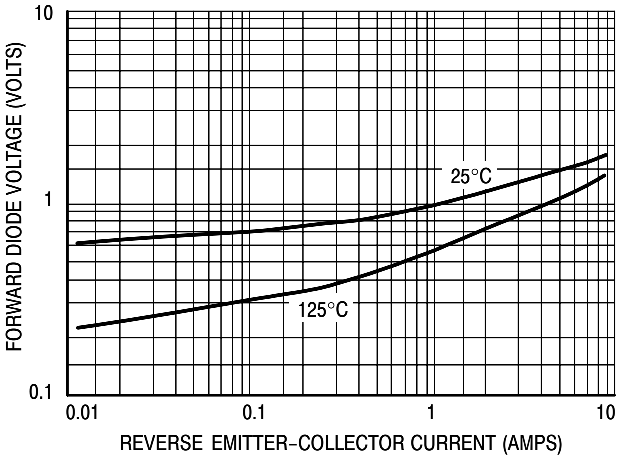


Figure 10. Forward Diode Voltage

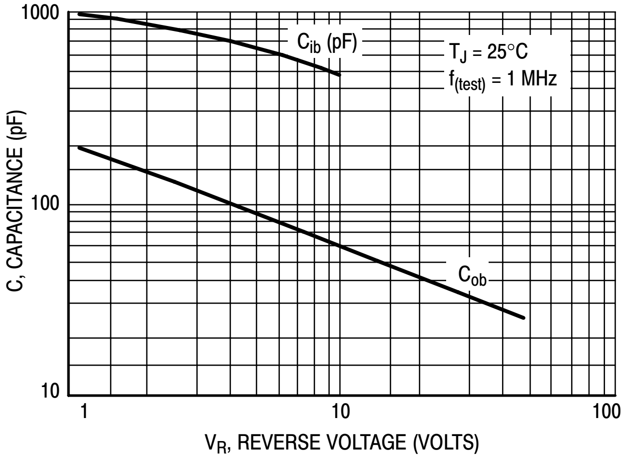


Figure 11. Capacitance

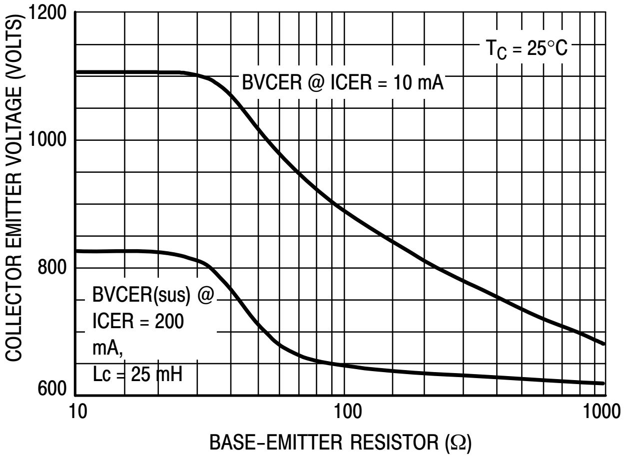


Figure 12. BVCER = f(R_{BE})

TYPICAL SWITCHING CHARACTERISTICS

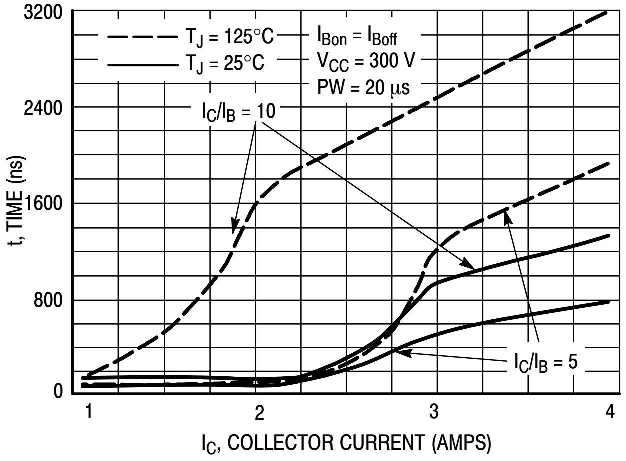


Figure 13. Resistive Switch Time, t_{on}

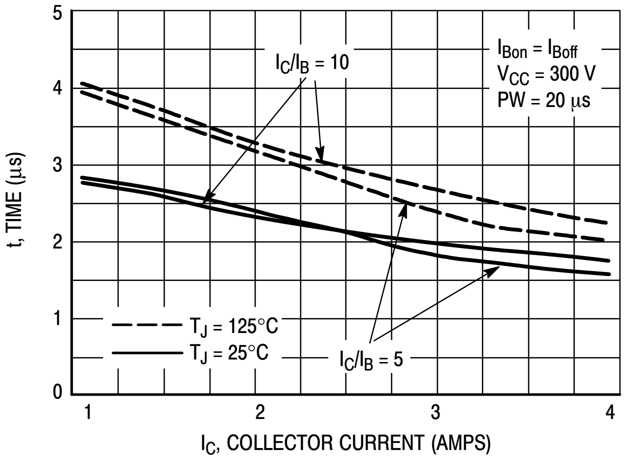


Figure 14. Resistive Switch Time, t_{off}

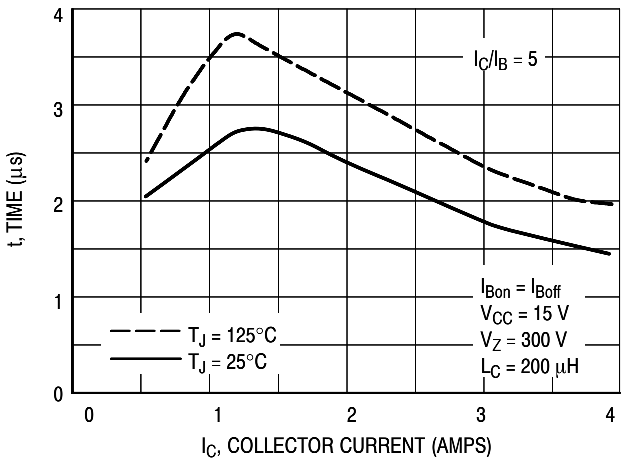


Figure 15. Inductive Storage Time, t_{si} @ $I_C/I_B = 5$

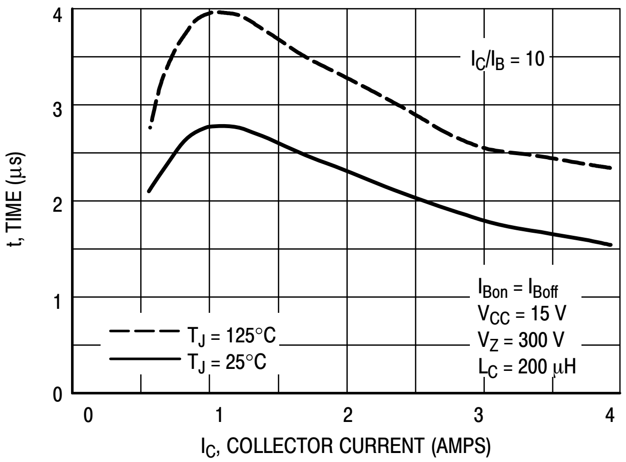


Figure 16. Inductive Storage Time, t_{si} @ $I_C/I_B = 10$

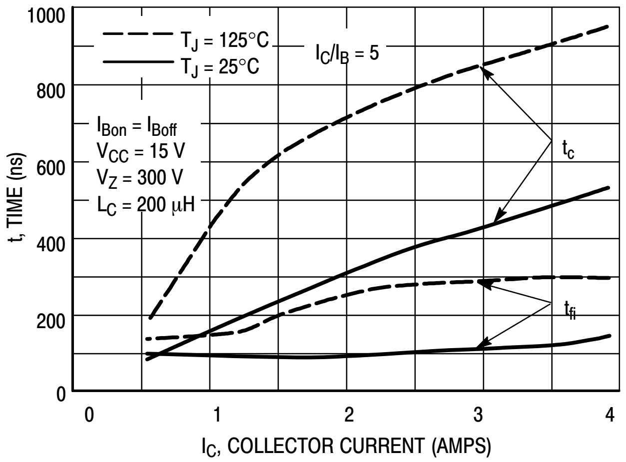


Figure 17. Inductive Switching Time, t_c and t_{fi} @ $I_C/I_B = 5$

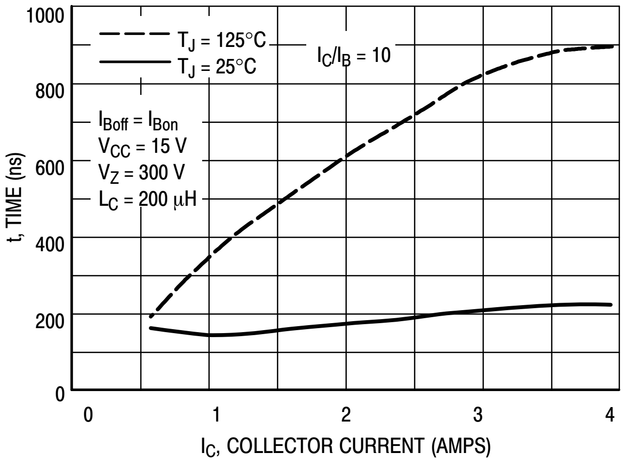


Figure 18. Inductive Switching Time, t_{fi} @ $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS

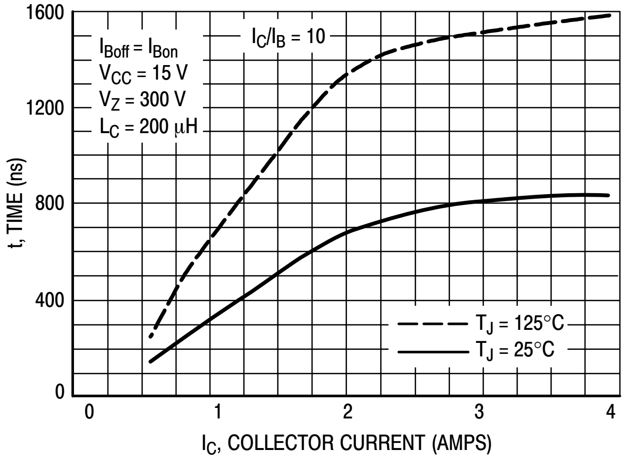


Figure 19. Inductive Switching, t_c @ $I_C/I_B = 10$

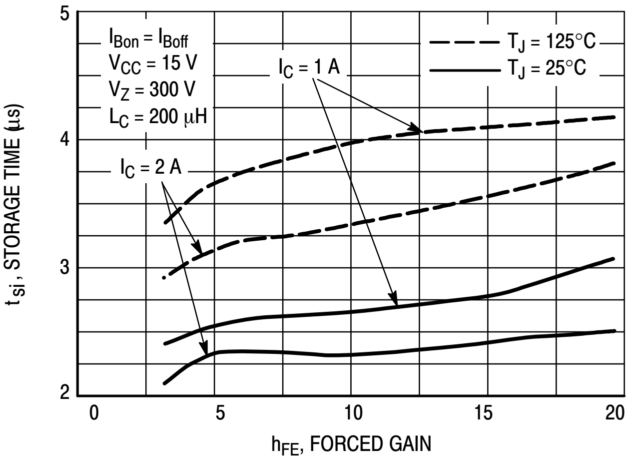


Figure 20. Inductive Storage Time

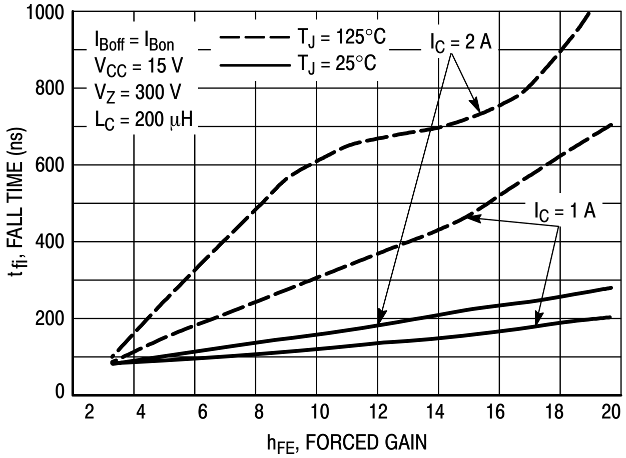


Figure 21. Inductive Fall Time

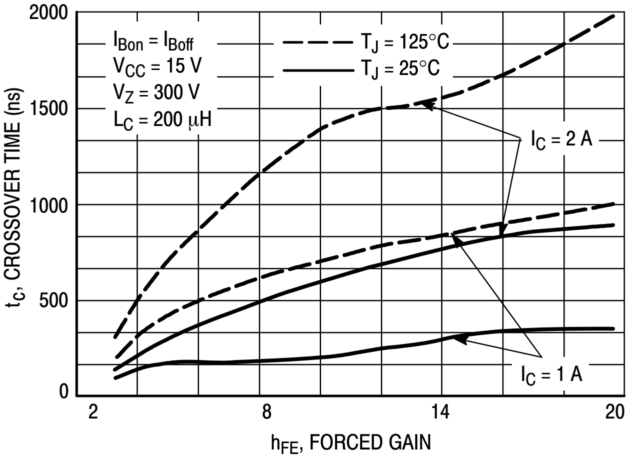


Figure 22. Inductive Crossover Time

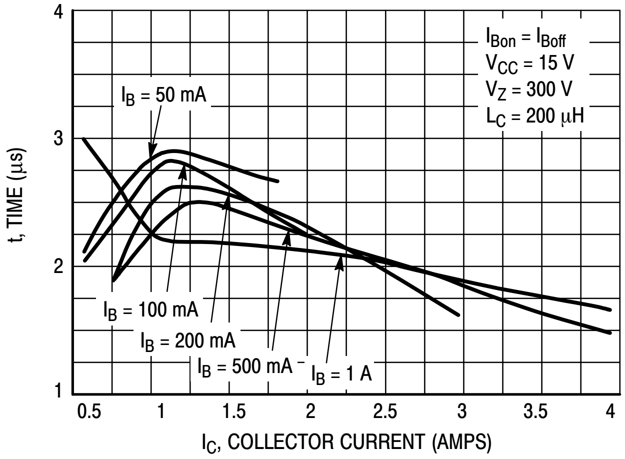


Figure 23. Inductive Storage Time, t_{si}

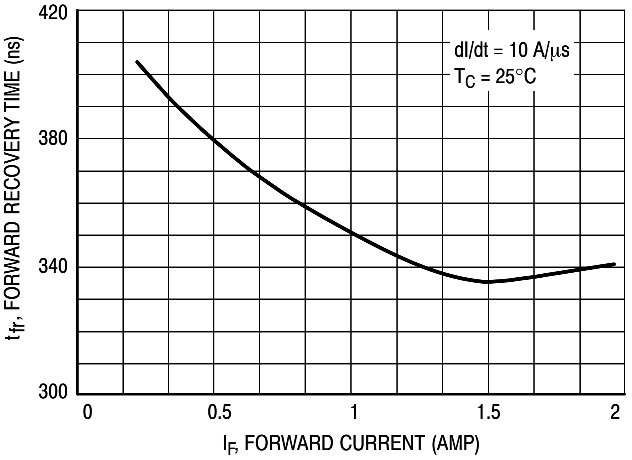


Figure 24. Forward Recovery Time, T_{FR}

TYPICAL SWITCHING CHARACTERISTICS

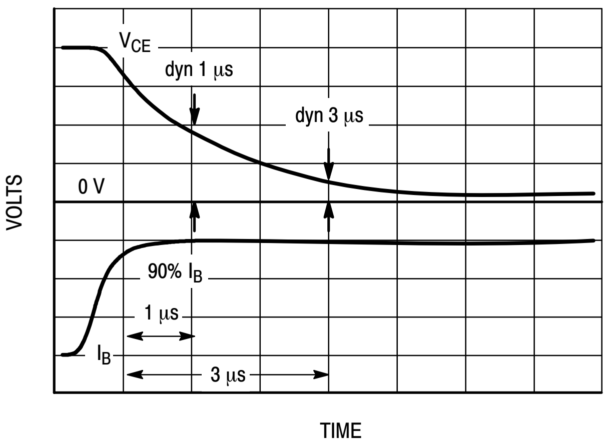


Figure 25. Dynamic Saturation Voltage Measurements

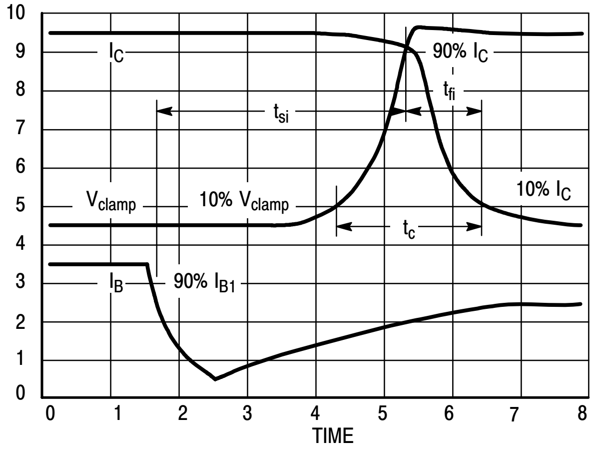


Figure 26. Inductive Switching Measurements

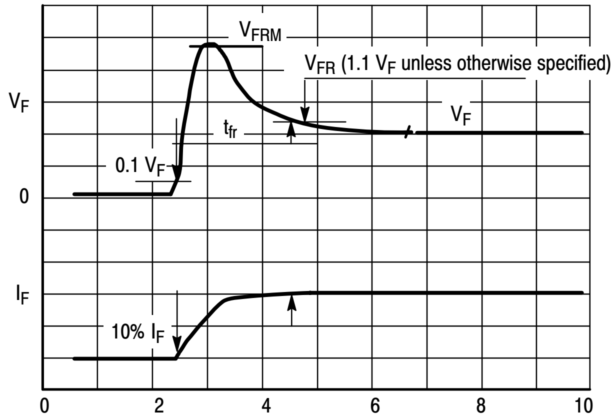
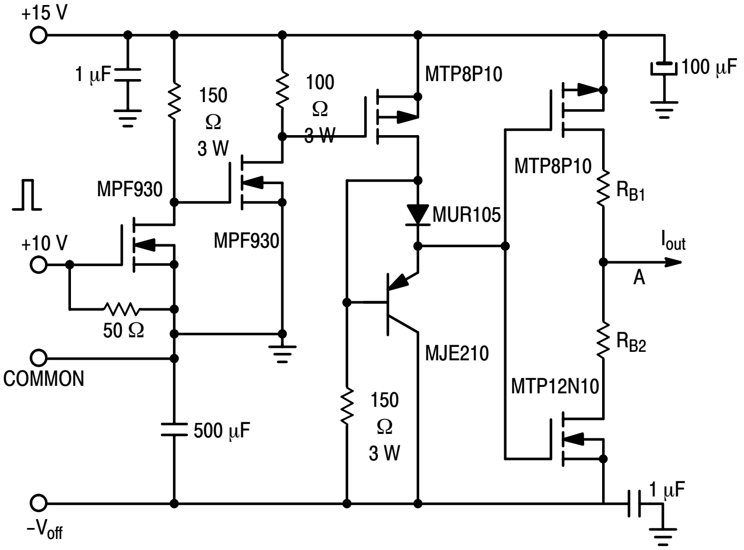
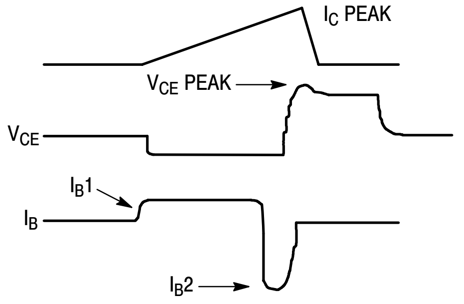


Figure 27. t_{fr} Measurements





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 V	V_{CC} = 15 V	V_{CC} = 15 V
$I_{C(pk)}$ = 100 mA	RB1 selected for desired Ib1	RB1 selected for desired Ib1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL CHARACTERISTICS

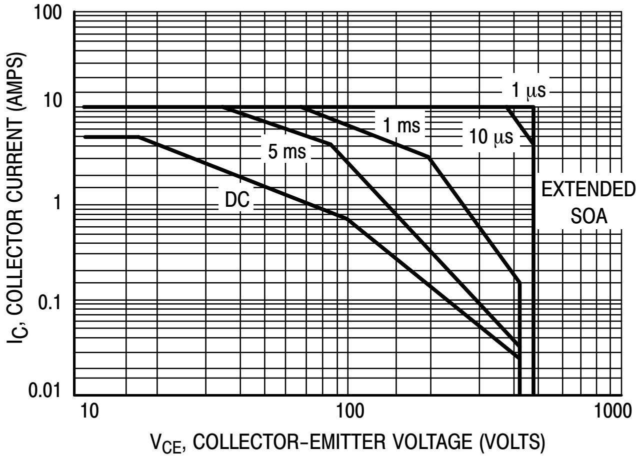


Figure 28. Forward Bias Safe Operating Area

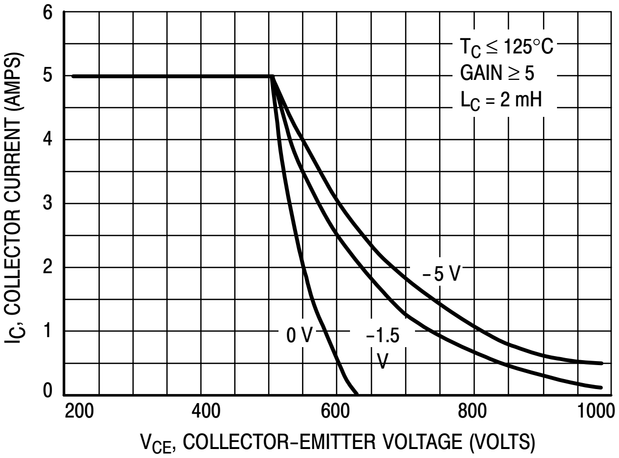


Figure 29. Reverse Bias Safe Operating Area

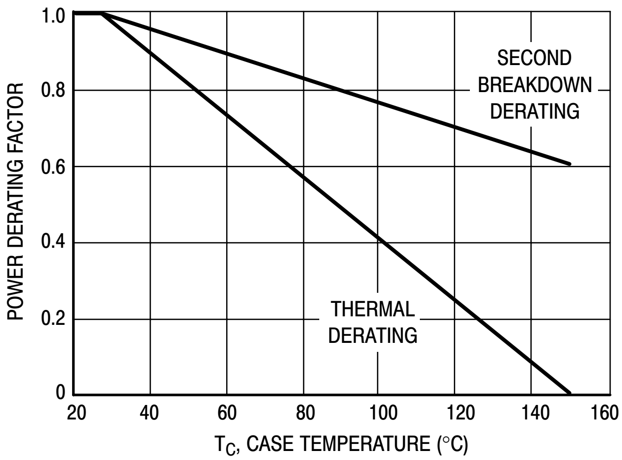


Figure 30. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C−V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

T_J(pk) may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn−off with the base−to−emitter junction reverse biased. The safe level is specified as a reverse−biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

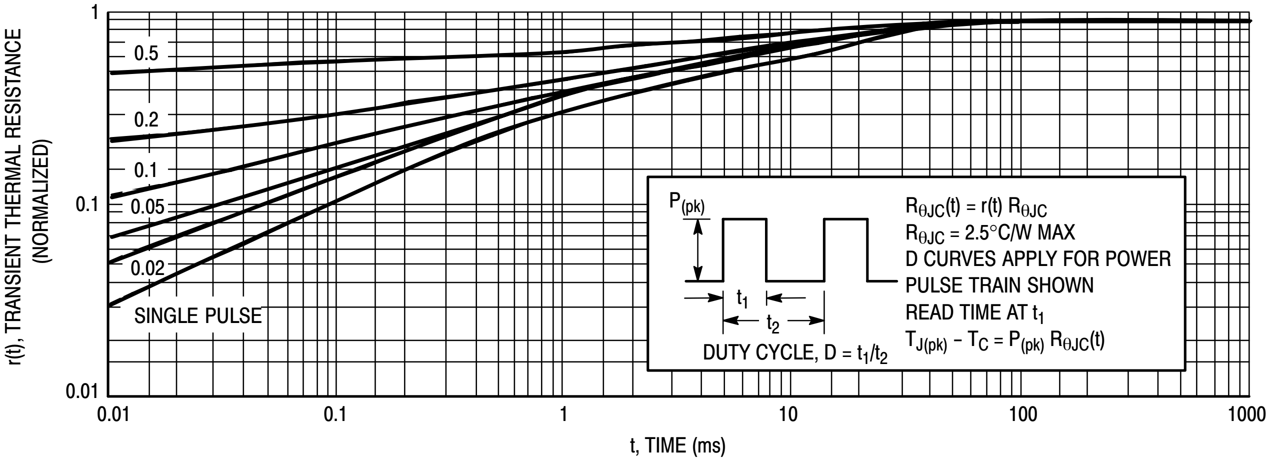
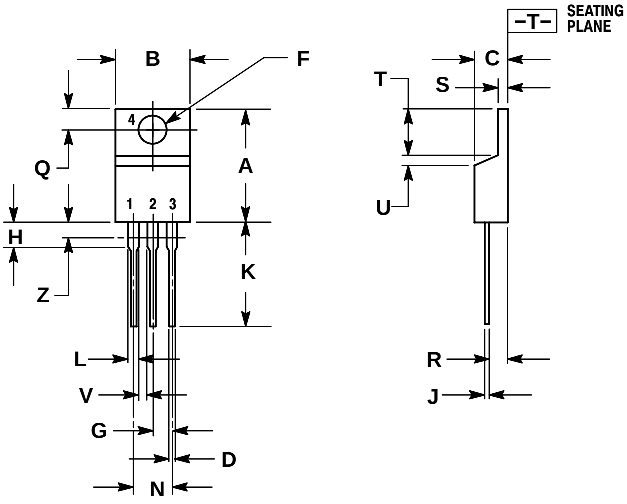


Figure 31. Typical Thermal Response ($Z_{\theta JC(t)}$) for MJE18004D2

PACKAGE DIMENSIONS

TO−220AB
CASE 221A−09
ISSUE AD



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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